## REMARKS

Claims 1-25 are pending. No new matter is presented.

Claims 23-25 were rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. In particular, the Examiner noted the claim 23 recites a "format adapter" which "is not described in the specification as a separate discrete element involved in the storage of compressed audio signals."

Claims 23-25 are supported by an enabling disclosure as required by Section 112, first paragraph. Claim 23 does not require the format adapter to be a separate discrete element, so there is nothing that requires the specification to describe the format adapter as a separate discrete element. Instead, claim 23 simply states that the non-volatile memory unit includes a format adapter and claim 1, from which claim 23 depends, indicates that the non-volatile memory unit is integrated in the chip. The specification supports such language by stating that the non-volatile memory 5 is embedded in the chip 50 and includes an interface circuit that "adapts the format of blocks or packets of data …" (page 4, line 22 – page 5, line 2; Figure 1). Accordingly, claims 23-25 are supported by an enabling disclosure.

One embodiment of the present invention provides an electronic device for the recording/reproduction of voice data that is entirely integrated in a chip of semiconductor material. It should be emphasized that the components of the electronic device, including the main transmission line, control unit, signal-conversion unit and non-volatile memory unit, are *all integrated in the same chip*. The advantages of this single-chip integration include a smaller device size and reduced power consumption. In addition, the unique architecture of the single-chip integration enables the device to optimize editing of the voice messages itself. Furthermore, the embodiment is characterized by the ability to accept and emit audio signals according to different formats by virtue of an interface circuit. This interface circuit adapts the format of data exchanged between the signal-conversion unit and the memory unit and implements a strategy of recovery of commands lost or failed.

Claims 1-3 and 23-25 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,694,200 to ("Naim").

Naim does not disclose the invention recited in claim 1. Claim 1 recites "An electronic device for the recording/reproduction of voice data, comprising: a chip of

semiconductor material; a main transmission line *integrated in said chip*; a control unit *integrated in said chip…*; a signal-conversion unit *integrated in said chip*; and a non-volatile memory unit *integrated in said chip…*" (Emphasis added). Like the Walters, Swingle, and Norris references, Naim does not disclose such elements *integrated in the same chip of semiconductor material*. Instead, Naim discloses in the DSP 4, DAC 20, ADC 21, and memory 8 as discrete components in Figures 1B (see col. 6, lines 14-23).

The applicants disagree with the Examiner's assertion that the paragraph at col. 4, lines 56-67 of Naim discloses a single chip of semiconductor material. That paragraph of Naim recites that the playing/recording player and the hard disk can be incorporated into a single housing or a single substrate, but such a housing and substate are not disclosed a being a single chip of semiconductor material. Instead, Naim clearly refers to the single substrate as being a single printed circuit board (PCB) 14 rather than a single semiconductor chip (see col. 7, lines 51-55 and Fig. 3). As is well known, such a housing or PCB 14 is not a single chip of semiconductor material. Instead, as is well known, a "chip" of semiconductor material is a single crystal of semiconductor material.

For the foregoing reasons, claim 1 is not anticipated by Naim.

Claims 2-3 and 23 depend on claim 1, and thus, also are not anticipated by Naim.

In addition, claim 23 recites other features that are not disclosed by Naim. In particular, claim 23 recites that the non-volatile memory unit includes a format adapter for adapting the format of the first stream of compressed digital signal for the non-volatile memory unit. Naim does mentions such a format adapter and such a format adapter is not inherent in the memory 8 of Naim. First, an unsupported conclusion that the memory 8 contained a format adapter does not satisfy the Examiner's burden of showing a specific teaching in the prior art of each claim element. In re Glaug, 283 F.3d 1335, 1341-1342 (Fed. Cir. 2002) (copy attached to September 8, 2005 Amendment). Second, nothing in the function or structure of Naim's system inherently requires the memory 8 to include a format adapter. The output of the DSP 4 and the ADC 21 could be in a format that is already compatible with the memory 8, and thus, there would be no need for the memory 8 to include a format adapter. Third, the underlying structure of the memory 8 could be designed to be compatible with the signals from the DSP 4 and ADC 21 without needing a particular format adapter.

Thus, claim 23 is in condition for allowance.

Naim does not disclose the invention recited in claims 24 and 25, which depend on claims 12 and 15, respectively. With respect to claims 12 and 15, the Examiner admitted that "Naim does not disclose that the signal-conversion unit has temporary storage means coupled to a converter circuit" (page 3, last two lines of Office Action). Accordingly, Naim cannot anticipate claims 24-25. In addition, although the language of claims 24-25 is not identical to that of claim 23, the novelty of claims 24-25 will be apparent in view of the above discussion of claim 23.

Claims 4-5 and 12-13 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Naim in view of Unno et al., EP 0 851 423 A1 ("Unno").

Naim and Unno do not teach or suggest the invention recited in claims 4 and 5, which depend on claim 1. Unno does not disclose anything about a single-chip integrated electronic device as recited in claim 1. Therefore, because Naim does not include all of the recited elements of claim 1, modifying Naim by incorporating the teachings of Unno (a buffer memory) would not satisfy the limitations of claims 4 and 5. Accordingly, claims 4-5 are nonobvious in view of the cited prior art.

Although the language of claims 12-13 and 15-16 is not identical to that of claims 4-5, the nonobviousness of claims 12-13 and 15-16 will be apparent in view of the above discussion.

Claims 6 and 7 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Naim and Unno in view of U.S. Patent No. 5,787,445 to Daberko.

The cited prior art references do not teach or suggest the invention recited in claims 6 and 7, which depend from claim 1. Daberko does not disclose anything about a single-chip integrated electronic device as recited in claim 1. Therefore, because the teachings of Naim and Unno do not include all of the recited elements of claim 1, modifying those teachings by incorporating the teachings of Daberko (first and second cache memories) would not satisfy the limitations of claims 6 and 7. Accordingly, claims 6-7 are nonobvious in view of the cited prior art.

Claims 8, 14, and 17-19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Naim and Unno in view of U.S. Patent No. 6,016,522 to Rossum.

The cited prior art references do not teach or suggest the invention recited in claim 8, which depends from claim 1. Rossum does not disclose anything about a single-chip integrated electronic device as recited in claim 1. Therefore, because the teachings of Naim and Unno do not include all of the recited elements of claim 1, modifying those teachings by incorporating the teachings of Rossum ("ping-pong" buffering) would not satisfy the limitations of claim 8. Accordingly, claim 8 is nonobvious in view of the cited prior art.

Although the language of claims 14 and 17-19 is not identical to that of claim 8, the nonobviousness of claims 14 and 17-19 will be apparent in view of the above discussion.

Claims 9-11 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Naim in view of U.S. Patent No. 6,604,168 to Ogawa.

Naim and Ogawa do not teach or suggest the invention recited in claims 9-11. Ogawa does not disclose anything about a single-chip integrated electronic device as recited in claim 1. Therefore, because the teachings of Naim does not include all of the recited elements of claim 1, modifying those teachings by incorporating the teachings of Ogawa (flash EEPROM management system) would not satisfy the limitations of claims 9-11. Accordingly, claims 9-11 are nonobvious in view of the cited prior art.

Claims 20-22 were rejected under 35 U.S.C. § 103 as being unpatentable over Naim and Unno in view of Ogawa. As discussed above Unno and Ogawa do not teach anything about a single-chip integrated electronic device as recited in claim 15, from which claims 20-22 depend. Accordingly, claims 20-22 are nonobvious in view of the cited prior art.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

SEED Intellectual Property Law Group PLLC

/Robert Iannucci/
Robert Iannucci
Registration No. 33,514

RXI:vsj

701 Fifth Avenue, Suite 6300
Seattle, Washington 98104-7092
Phone: (206) 622-4900 / Fax: (206) 682-6031
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